

## IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-28. (Canceled)

1           29.   (New) A program storage device readable by a computer, the program  
2   storage device tangibly embodying one or more programs of instructions executable by  
3   the computer to perform operations for determining when to perform an error recovery  
4   instruction, the operations comprising:  
5           receiving an error recovery instruction;  
6           beginning a timeout task;  
7           monitoring a processor interface to identify processor status for determining a  
8   time to perform the error recovery instruction for withholding access to the local  
9   processor; and  
10          performing the error recovery instruction when the monitoring determines a  
11   time for performing the error recovery instruction.

1           30.   (New) The program storage device of claim 28 further comprising  
2   forcing an execution of the error recovery instruction when the timeout task expires  
3   before the monitoring determines a time to perform the error recovery instruction.

1           31.   (New) The program storage device of claim 30 further comprising  
2   resuming normal operations after performing the error recovery instruction.

1           32.   (New) The program storage device of claim 28, wherein the monitoring  
2   a processor interface to identify processor status for determining a time to perform the  
3   error recovery instruction for withholding access to the local processor further  
4   comprises:  
5           monitoring a processor interface to a host bus for an idle condition;  
6           withholding access to the processor interface when the idle condition is  
7   detected;  
8           after access to the processor interface is withheld, interrogating all data transfer  
9   paths to determine when all the data paths are idle; and  
10          identifying the time to perform the error recovery instruction when all data  
11   transfer paths are idle.

1           33.   (New) The program storage device of claim 32 further comprising  
2   resuming normal operations after performing the error recovery instruction.

1           34.   (New) The program storage device of claim 28 further comprising  
2   resuming normal operations after performing the error recovery instruction.

1           35.   (New) A program storage device readable by a computer, the program  
2 storage device tangibly embodying one or more programs of instructions executable by  
3 the computer to perform operations for determining when to perform an error recovery  
4 instruction, the operations comprising:  
5           receiving an error recovery instruction;  
6           monitoring a processor interface to identify processor status for determining a  
7 time to perform the error recovery instruction for withholding access to the local  
8 processor; and  
9           performing the error recovery instruction when the monitoring determines a  
10 time for performing the error recovery instruction.

1           36.   (New) The program storage device of claim 35 further comprising  
2 beginning a timeout task after receiving the error recovery instruction and forcing an  
3 execution of the error recovery instruction when the timeout task expires before the  
4 monitoring determines a time to perform the error recovery instruction.

1           37.   (New) The program storage device of claim 36 further comprising  
2 resuming normal operations after performing the error recovery instruction.

1           38.   (New) The program storage device of claim 35, wherein the monitoring  
2   a processor interface to identify processor status for determining a time to perform the  
3   error recovery instruction for withholding access to the local processor further  
4   comprises:  
5           monitoring a processor interface to a host bus for an idle condition;  
6           withholding access to the processor interface when the idle condition is  
7   detected;  
8           after access to the processor interface is withheld, interrogating all data transfer  
9   paths to determine when all the data paths are idle; and  
10          identifying the time to perform the error recovery instruction when all data  
11   transfer paths are idle.

1           39.   (New) The program storage device of claim 38 further comprising  
2   resuming normal operations after performing the error recovery instruction.

1           40.   (New) The program storage device of claim 35 further comprising  
2   resuming normal operations after performing the error recovery instruction.

1           41.   (New) An apparatus for quiescing processor control logic upon receipt  
2 of an error recovery instruction, comprising:  
3           self-quiesce logic for receiving an error recovery instruction; and  
4           a timer, coupled to the self-quiesce logic, for determining when to force  
5 execution of the error recovery instruction;  
6           wherein the self-quiesce logic initiates the timer when the error recovery  
7 instruction is received, begins to monitor a processor interface to identify processor  
8 status for determining a time to perform the error recovery instruction for withholding  
9 access to the local processor and performs the error recovery instruction when the  
10 monitoring determines a time for performing the error recovery instruction.

1           42.   (New) The apparatus of claim 41, wherein the self-quiesce logic forces  
2 an execution of the error recovery instruction when the timer expires before the self-  
3 quiesce logic determines a time to perform the error recovery instruction.

1           43.   (New) The apparatus of claim 42, wherein the self-quiesce logic allows  
2 resuming normal operations after the error recovery instruction is performed.

1           44.   (New) The apparatus of claim 41, wherein the self-quiesce logic  
2   monitors a processor interface to a host bus to identify processor status for determining  
3   a time to perform the error recovery instruction for withholding access to the local  
4   processor by monitoring the processor interface for an idle condition, withholding  
5   access to the processor interface when the idle condition is detected, after access to the  
6   processor interface is withheld, interrogating all data transfer paths to determine when  
7   all the data paths are idle and identifying the time to perform the error recovery  
8   instruction when all data transfer paths are idle.

1           45.   (New) The apparatus of claim 44, wherein the self-quiesce logic allows  
2   resuming normal operations after the error recovery instruction is performed.

1           46.   (New) The apparatus of claim 41, wherein the self-quiesce logic allows  
2   resuming normal operations after the error recovery instruction is performed.

1           47.   (New) An apparatus for quiescing processor control logic upon receipt  
2 of an error recovery instruction, comprising:  
3           a processor for executing instructions; and  
4           self-quiesce logic, coupled to the processor, the self-quiesce logic detecting an  
5 error recovery instruction, wherein the self-quiesce logic monitors a processor interface  
6 to identify processor status for determining a time to perform the error recovery  
7 instruction for withholding access to the local processor and performs the error  
8 recovery instruction when the monitoring determines a time for performing the error  
9 recovery instruction.

1           48.   (New) The apparatus of claim 47 further comprising a timer for  
2 determining when to abort the monitoring of processor status and data path activity and  
3 cause an execution of the error recovery instruction.

1           49.   (New) The apparatus of claim 48, wherein the self-quiesce logic causes  
2 normal operations to be resumed after performing the error recovery instruction.

1           50.     (New) The apparatus of claim 47, wherein the self-quiesce logic  
2     monitors a processor interface to a host bus to identify processor status for determining  
3     a time to perform the error recovery instruction for withholding access to the local  
4     processor by monitoring the processor interface for an idle condition, withholding  
5     access to the processor interface when the idle condition is detected, after access to the  
6     processor interface is withheld, interrogating all data transfer paths to determine when  
7     all the data paths are idle and identifying the time to perform the error recovery  
8     instruction when all data transfer paths are idle.

1           51.     (New) The apparatus of claim 50, wherein the self-quiesce logic causes  
2     normal operations to be resumed after performing the error recovery instruction.

1           52.     (New) The apparatus of claim 47, wherein the self-quiesce logic causes  
2     normal operations to be resumed after performing the error recovery instruction.



1           53.   (New) A method for determining when to perform an error recovery  
2 instruction, comprising:  
3           receiving an error recovery instruction;  
4           beginning a timeout task;  
5           monitoring a processor interface to identify processor status for determining a  
6 time to perform the error recovery instruction for withholding access to the local  
7 processor; and  
8           performing the error recovery instruction when the monitoring determines a  
9 time for performing the error recovery instruction.

1           54.   (New) A method for determining when to perform an error recovery  
2 instruction, comprising:  
3           receiving an error recovery instruction;  
4           monitoring a processor interface to identify processor status for determining a  
5 time to perform the error recovery instruction for withholding access to the local  
6 processor; and  
7           performing the error recovery instruction when the monitoring determines a  
8 time for performing the error recovery instruction.

1           55.   (New) An apparatus for quiescing processor control logic upon receipt  
2 of an error recovery instruction, comprising:  
3           means for receiving an error recovery instruction; and  
4           means for determining when to force execution of the error recovery instruction;  
5           wherein the means for receiving the error recovery instruction initiates a timer  
6 when the error recovery instruction is received, begins to monitor a processor interface  
7 to identify processor status for determining a time to perform the error recovery  
8 instruction for withholding access to the local processor and performs the error  
9 recovery instruction when a time for performing the error recovery instruction is  
10 determined.

1           56.   (New) An apparatus for quiescing processor control logic upon receipt  
2 of an error recovery instruction, comprising:  
3           means for executing instructions; and  
4           means, coupled to the means for executing instructions, for detecting an error  
5 recovery instruction, monitoring a processor interface to identify processor status for  
6 determining a time to perform the error recovery instruction for withholding access to  
7 the local processor and performing the error recovery instruction when a time for  
8 performing the error recovery instruction is determined.